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1. **Generation of design verification tests from behavioral VHDL programs using path and constraint programming**

Vemuri, R.; Kalyanaraman, R.

[Very Large Scale Integration \(VLSI\) Systems, IEEE Transactions on](#)

Volume: 3 Issue: 2 Jun 1995

Page(s): 201-214

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**Summary:** A method for generation of design verification tests from behavior-level VHDL is presented. The method generates stimuli to execute desired control-flow paths in the target program. This method is based on path enumeration, constraint ge.....

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